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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/938,237
Filing Date: August 23, 2001
Appellant(s): PLATTETER ET AL.

John S. Zanghi
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed April 28, 2005.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection in the brief is correct.

Non-Appealable Issues

Appellant's brief presents arguments relating to the propriety of the final rejection. This issue relates to petitionable subject matter under 37 CFR 1.181 and not to appealable subject matter. See MPEP § 1002 and § 1201.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

The following is a listing of the evidence (e.g., patents, publications, Official Notice, and admitted prior art) relied upon in the rejection of claims under appeal.

U.S. Patent 5,995,771	Miyawaki	11-1999

U.S. Patent 4,807,259	Yamanaka et al.	2-1989
U.S. Patent 6,675,249	Shimoda et al.	1-2004
U.S. Patent 6,343,351	Lackman et al.	1-2002
U.S. Patent 6,704,302	Einbinder et al.	3-2004
U.S. Patent 5,535,217	Cheung et al.	7-1995

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

4. The following are fact findings for support of all rejections in the instant Office Action.

4.1. Yamanaka discloses a document processing system [master station 1 comprises typewriter 13 for document processing][1].

4.2. Yamanaka discloses the system comprises a controller [master station 1], including a master clock [17] and logic [CPU 10 and code sending and receiving circuit 18] for generating a discrete clock synchronization interrupt signal [S11; col.7, ll.6-8; being utilized in a synchronization process, S11 is an interrupt signal requiring the receiving station to act on the signal within an acceptable time of tp – col.7, ll.17-20].

4.3. Yamanaka discloses the system comprises a resource [slave station 2], including a slave clock [27] related to operational timing of the resource [the slave station utilizes a slave clock to provide timing functionality to slave station components such as CPU 20 which inherently, requires a local timing input] and circuitry for receiving and processing the discrete clock

synchronization interrupt signal [code sensing and receiving circuit 28 and CPU 20; col.3, ll.5-11; col.7, ll.12-17].

4.4. Yamanaka discloses the system comprises a control bus [data transmission path 5], interconnecting the resource and the controller, for distributing the discrete interrupt signal [col.2, ll.25-28; col.4, ll.20-22].

4.5. Yamanaka discloses the resource circuitry includes a processor [CPU 20] for adjusting the slave clock to provide for compatibility with the controller [col.7, ll.42-47].

4.6. Yamanaka discloses the system includes a plurality of resources [slave stations 2 and 3], each resource including a slave clock [27 and 37] related to operational timing of the resource and circuitry for receiving and processing the clock synchronization interrupt signal [code sending and receiving circuit 28 and 38, CPU 20 and 30].

4.7. Yamanaka discloses the control bus [data transmission path 5] interconnects each resource with the controller thereby distributing the interrupt signal to each resource [col.2, ll.25-28; col.4, ll.20-22].

4.8. Yamanaka discloses the circuitry in each resource includes a processor [CPU 20 and 30] for adjusting the slave clock associated with the resource to provide for compatibility with the controller [col.7, ll.42-47].

4.9. Yamanaka discloses the system comprises a plurality of resources [slave stations 2 and 3], each resource including a slave clock [27 and 37] related to operational timing of the resource and logic for receiving the discrete interrupt signal [code sending and receiving

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[1] Although there are several embodiments, the pertinent reference items generally have the same functionalities and do not contradict one another [col.6, ll.37-41, ll.53-55].

circuit 28 and 38], processing the discrete interrupt signal [CPU 20 and 30], and synchronizing the slave clock with the master clock [col.7, ll.42-47].

4.10. Yamanaka discloses the system comprises electrical wiring [data transmission path 5] interconnecting the resources and the controller for distributing the discrete interrupt signal to the resources [col.2, ll.25-28; col.4, ll.20-22].

4.11. Yamanaka discloses the resources include one or more finishing devices [output circuit 24].

4.12. Yamanaka discloses the resources include one or more feeding devices [input circuit 25].

4.13. Yamanaka discloses a document processing system comprising a plurality of resources [slave stations 2 and 3] [col.7, ll.3-5].

4.14. Yamanaka discloses a method of initially synchronizing the slave clock with the master clock [abstract].

4.15. Yamanaka discloses the method comprising saving a value of the master clock in the controller [col.7, ll.9-11].

4.16. Yamanaka discloses the method comprising generating a discrete clock synchronization interrupt signal in the controller and distributing the discrete interrupt signal to the resource via the control bus [col.7, ll.6-8].

4.17. Yamanaka discloses the method comprising receiving the discrete interrupt signal at the resource and saving a first value of the slave clock [col.7, ll.12-17].

4.18. Yamanaka teaches the advantage of synchronizing the master and slave clocks within a range of error in order to avoid problems for practical use [col.1, ll.56-59].

4.19. Cheung et al., U.S. Patent 5535217, hereinafter Cheung, discloses a system for synchronizing a master and slave clocks [col.1, ll.8-12].

4.20. Cheung discloses the resource circuitry includes a processor [CPU 202] for determining the compatibility of the slave clock with the master clock [FIG.12; col.3, ll.2-5; col.5, ll.45-53].

4.21. Cheung discloses the compatibility between the resource and the controller is such that the slave clock is synchronized to within one clock cycle of the master clock [col.4, ll.37-41; set the precision values such as Q and restrict the transmission times appropriately].

4.22. Cheung discloses a method for synchronizing a controller [master or process B] and resource [slave or process A] clocks [col.1, ll.8-12].

4.23. Cheung discloses the method comprising saving a first value [time T] of the slave clock [col.4, ll.6-7].

4.24. Cheung discloses the method comprising sending a message from the resource to the controller via the network to request the value [time U] saved for the master clock [col.2, ll.66-67; col.4, ll.8-10].

4.25. Cheung discloses the method comprising sending the value saved for the master clock from the controller to the resource via the network [col.2, l.67 to col.3, l.2; col.4, ll.11-12].

4.26. Cheung discloses the method comprising receiving the value saved for the master clock at the resource [col.2, l.2; col.4, l.12].

4.27. Cheung discloses the method comprising saving a second value of the slave clock [time V] in the resource [col.2, ll.2-3; col.4, ll.13-14].

4.28. Cheung discloses the method comprising subtracting the first value [time T] from the second value [time V] to determine a slave clock difference value [V-T] [col.4, ll.30-32].

4.29. Cheung discloses the method comprising adding the difference value [V-T] to the value saved for the master clock [U] to determine a synchronized value for [U+V-T] the slave clock and setting the slave clock to the synchronized value [col.4, ll.37-41; Q=0].

4.30. Cheung discloses the method comprising subtracting the value saved for the slave clock [time T] from the value saved for the master clock [time U] to determine an error value between the slave clock and the master clock [U-T] and using the error value in an adjustment algorithm to adjust the slave clock to be synchronized with the master clock [col.4, ll.37-41; utilize V and Q in algorithm].

4.31. Cheung discloses the method wherein the periodic interval for performing the steps [a through g in application] during steady state operation of the document processing system is about two seconds [col.4, ll.37-41; with Q=0 and ignoring calculation time assumed to be insignificant, focus on the more significant transmission time if that be the case so that the algorithm involving Q, V, and T would yield 2].

4.32. Cheung teaches that the advantage of using the round trip clock synchronization scheme as taught by Cristian can provide further precision tuning [col.3, ll.23-31] and enhance the accuracy of the network synchronization results [col.2, ll.47-52].

4.33. Shinoda et al., U.S. Patent 6675249, hereinafter Shinoda, discloses an information processing system with a processor for determining the compatibility of a plurality of clocks [col.7; ll.49-50].

4.34. Lackman et al., U.S. Patent 6343351, hereinafter Lackman, discloses a data processing system providing hard real-time service [col.3, ll.24-32].

4.35. Lackman teaches the advantage of providing hard real-time service is the prevention of catastrophic results in critical systems due to data loss [col.3, ll.29-32].

4.36. Einbinder et al., U.S. Patent 6704302, hereinafter Einbinder, discloses a 10 base T network for connecting workstations [col.3, ll.4-19].

4.37. Kurd et al., U.S. Patent 6320424, hereinafter Kurd, discloses the synchronization of a clock during steady state operation [col.8, ll.10-12; col.9, ll.20-24].

4.38. Miyawaki, U.S. Patent 5995771, discloses a document processing system [image forming administration system] [fig.1].

4.39. Miyawaki discloses the system comprising a marking engine that marks a sheet to form at least a portion of a document [copier], the marking engine including a controller [control unit] [col.3, ll.54-63].

4.40. Miyawaki discloses the system comprising a resource that transfers the sheet to the marking engine [feeder] or receives the sheet from the marking engine [finisher] [col.4, ll.8-11].

4.41. Miyawaki discloses the system comprising a control bus [system bus 18], interconnecting the resource and the controller [col.4, ll.8-11, ll.35-39].

5. Yamanaka, Cheung, Shinoda, Lackman, Eibinder, and Kurd were cited as prior art in the previous Office Action.

Re Claim 1, 3, 6-7, 10-11, and 21

6. Claims 1, 3, 6-7, 10-11, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyawaki in view of Yamanaka.

7. In re claim 1, Miyawaki discloses each and every limitation of the claim [findings 4.38-4.41]. Miyawaki did not discuss the details of synchronization between the controller of the marking engine and the resource. Yamanaka discloses a system comprising a controller, resource, and control bus with the synchronization details [findings 4.1-4.4]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the synchronization teachings of Yamanaka into the document processing system of Miyawaki in order to synchronize operations among the resources and controller of the marking engine. One of ordinary skill in the art would have been motivated to make such a combination in order to provide a way to synchronize operations for practical use [finding 4.18].

8. As to claim 3, see finding 4.5.

9. As to claim 6, see findings 4.6 and 4.7.

10. As to claim 7, see finding 4.8.

11. As to claim 10, see finding 4.11.

12. As to claim 11, see finding 4.12.

13. As to claim 21, see findings 4.2, 4.9 and 4.10.

Re Claim 2

14. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyawaki and Yamanaka, as applied to claim 1 above, and further in view of Shimoda.

15. In re claim 2, Yamanaka and Miyawaki disclose each and every limitation of the claim, as discussed above in reference to claim 1. Yamanaka and Miyawaki did not discuss the use of the

resource processor for determining the compatibility of the slave clock with the master clock. Shimoda teaches a processor for determining the compatibility of a plurality of clocks [finding 4.33] in order to provide synchronization. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the processor taught by Shimoda for determining the compatibility of the slave clock with the master clock in the resource circuitry disclosed by Yamanaka and Miyawaki as the processor taught by Shimoda is a known device for use in determining the compatibility between two values suitable for use as the processor of Yamanaka and Miyawaki. One of ordinary skill in the art would have been motivated to make such a combination in order to provide a mechanism for determining the compatibility between the two clocks for synchronization.

Re Claims 4 and 8

16. Claims 4 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyawaki and Yamanaka, as applied to claims 3 and 7 above, and further in view of Lackman.

17. In re claim 4, Miyawaki and Yamanaka disclose each and every limitation of the claim, as discussed above in reference to claim 3. Miyawaki and Yamanaka did not discuss the use of the compatibility between the resource and the controller to provide hard real-time service. Lackman teaches a data processing system providing hard real-time service [finding 4.34] to avoid catastrophic results due to data loss within a limited time frame [finding 4.35]. It would have been obvious to one of ordinary skill in the art, having the teachings of Miyawaki, Yamanaka and Lackman before him at the time the invention was made, to modify the clock synchronization system disclosed by Miyawaki and Yamanaka to include the hard real-time service as taught by Lackman, in order to provide a hard real-time clock synchronization system

[e.g., information from CPU 10 to CPU 20 must be received in a "fresh" state of no older than an X amount of clock cycles in order for system to function properly]. One of ordinary skill in the art would have been motivated to make such a combination in order to provide a mechanism for ensuring the safety of the system with critical operations that need to be serviced within a limited time frame.

18. As to claim 8, see finding 4.13 and discussion above in reference to claim 4.

Re Claim 12

19. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Miyawaki and Yamanaka, as applied to claim 6 above, and further in view of Einbinder.

20. In re claim 12, Miyawaki and Yamanaka disclose each and every limitation of the claim, as discussed above in reference to claim 6. Miyawaki and Yamanaka did not disclose expressly the use of a 10 base T network for interconnecting the resources and the controller. Einbinder teaches a 10 base T network for interconnecting nodes in a network to take advantage of the timing margins [finding 4.36]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the 10 base T network as taught by Einbinder to connect the resources and controller disclosed by Miyawaki and Yamanaka as the 10 base T taught by Einbinder is a known connecting device for use in the system of Miyawaki and Yamanaka. One of ordinary skill in the art would have been motivated to make such a combination in order to provide a mechanism for interconnecting the resources and controller with controllable timing margins for synchronization purposes.

Re Claims 5, 9, and 13-20

21. Claims 5, 9, and 13-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Miyawaki and Yamanaka, as applied to claims 1, 3, and 7 above, and further in view of Cheung.

22. In re claim 5, Miyawaki and Yamanaka disclose each and every limitation of the claim, as discussed above in reference to claim 3. Miyawaki and Yamanaka did not discuss the detail of the compatibility between the resource and the controller to be such that the slave clock is synchronized to within one clock cycle of the master clock. Cheung teaches a system for synchronizing a master and slave clocks [finding 4.19], wherein the compatibility between the resource and the controller is such that the slave clock is synchronized to within one clock cycle of the master clock [finding 4.21] in order to avoid problems for practical use [finding 4.18]. It would have been obvious to one of ordinary skill in the art, having the teachings of Miyawaki, Yamanaka and Cheung before him at the time the invention was made, to modify the system taught by Miyawaki and Yamanaka to include the synchronization mechanism as taught by Cheung, in order to obtain the compatibility between the resource and the controller such that the slave clock is synchronized to within one clock cycle of the master clock. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to synchronize the clocks within a range and avoid problems for practical use.

23. As to claim 9, see finding 4.13 and discussion above in reference to claim 5.

24. In re claim 13, Miyawaki and Yamanaka disclose each and every limitation of the claim as discussed above in reference to claim 1 [include findings 4.2-4.4 and 4.13-4.17]. Yamanaka did not address how the resource can improve the accuracy of the synchronization. Cheung teaches a system for synchronizing a master and slave clocks [finding 4.19]. Thus, Cheung teaches a system similar to that of Miyawaki and Yamanaka. Cheung further teaches the steps the resource

may take to synchronize its clock with the controller's master clock [findings 4.22-4.29] in order to increase the accuracy of the synchronization [finding 4.32]. It would have been obvious to one of ordinary skill in the art, having the teachings of Miyawaki, Yamanaka and Cheung before him at the time the invention was made, to modify the system taught by Miyawaki and Yamanaka to include the synchronization mechanism as taught by Cheung, in order to provide a way for the resource to increase the accuracy of synchronization. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase the accuracy of the synchronization.

25. As to claim 14, see finding 4.13 and discussion above in reference to claim 13.

26. In re claim 15, Miyawaki and Yamanaka discloses each and every limitation of the claim [findings 4.2-4.4 and 4.13-4.17]. Miyawaki and Yamanaka did not address how the resource can improve the accuracy of the synchronization. Cheung teaches a system for synchronizing a master and slave clocks [finding 4.19]. Thus, Cheung teaches a system similar to that of Miyawaki and Yamanaka. Cheung further teaches the steps the resource may take to synchronize its clock with the controller's master clock [findings 4.22-4.26 and 4.30] in order to increase the accuracy of the synchronization [finding 4.32]. It would have been obvious to one of ordinary skill in the art, having the teachings of Miyawaki, Yamanaka and Cheung before him at the time the invention was made, to modify the system taught by Miywaki and Yamanaka to include the synchronization mechanism as taught by Cheung, in order to provide a way for the resource to increase the accuracy of synchronization. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to increase the accuracy of the synchronization.

27. As to claim 16, see discussion above in reference to claim 5.

28. As to claim 17, see finding 4.37.

29. As to claim 18, see finding 4.31.

30. As to claim 19, see discussion above in reference to claim 14.

31. As to claim 20, see discussion above in reference to claim 9.

(10) Response to Argument

A. Rejection of Claims 1-21 and Finality of Rejection Does Not Provide Appellants With Fair Opportunity to Identify the Issues and Reply Because Examiner Has Not Properly Communicated the Basis for Rejection.

Appellant's arguments with respect to part A are moot. The propriety of the final Office Action is a petitionable issue.

B. Rejection of 'Claims 1-21 is Improper Because Examiner Has Not Properly Established Some Suggestion or Motivation to Combine Miyawaki and Yamanaka.

Appellant's arguments with respect to part B have been fully considered but they are not persuasive as detailed in the following.

Appellant asserts "Examiner has identified explicit motivation to combine Miyawaki and Yamanaka". Examiner agrees as explicit motivation is required to establish obviousness (MPEP 2143.01).

Appellant alleges "Miyawaki has nothing to do with clock synchronization nor is it ever mentioned in the patent... in fig.3 of Miyawaki there is shown an interrupt signal... Miyawaki most closely refers to a concept that is called 'cluster printing..." In response to Appellant's arguments against the references individually, one cannot show nonobviousness by attacking

references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). As indicated in part 6 of the Final Rejection, claims 1, 3, 6-7, 10-11, and 21 were rejected based on a combination of Miyawaki in view of Yamanaka. That is, the fact findings for Miyawaki [4.38-4.41], clearly written in claims language to match the pertinent limitations of claims 1, 3, 6-7, 10-11, and 21, do not discuss clock synchronization *because* ***Yamanaka*** *is relied upon for such teachings.*

Appellant further argues that Miyawaki is nonanalogous art. It has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Examiner submits that both Miyawaki and Appellant are involved in the field associated with document processing system [i.e., copiers with controllers and resources].

Appellant argues that Miyawaki "has nothing to do with clock synchronization". The Examiner disagrees and respectfully submits that Miyawaki's document processing system comprising of various independent modules [e.g., copiers, finishers, feeders, CPU, i/o ports] would require synchronization in order to operate properly. For example, the resources of feeders/finishers disclosed by Miyawaki are independent modules controlled by a copier control unit that perform independent operations of transferring/receiving the sheets to/from the copier [col.4, ll.8-11]. Examiner submits that in order to be of practical use, a transfer of sheet must be done before the copier actually imprints any image, and the imprinting must be completed before

the sheet is to be received. If any of the operations were out of synchronized order, there would be no imprinted image on a sheet. Further, Examiner submits that the data latching required amongst the independent modules during communication may require clock synchronization. Thus, it would be more proper to assert, as Examiner did in part 7 of the Final Rejection, that "Miyawaki did not discuss *the details of synchronization*".

Appellant asserts that "in order for the Examiner to establish a prima facie case of obviousness for claim 1, Yamanaka must disclose the details of synchronization that are not discussed in Miyawaki". Examiner agrees as indicated in part 6 of the Final Rejection, claims 1, 3, 6-7, 10-11, and 21 were rejected based on a combination of Miyawaki in view of Yamanaka. That is, the fact findings for Miyawaki [4.38-4.41] and Yamanaka [4.1-4.12], clearly written in claims language to match the pertinent limitations of claims 1, 3, 6-7, 10-11, and 21, demonstrates ***Yamanaka** is relied upon for teaching the details of synchronization.*

Appellant asserts that "Examiner found explicit motivation to combine Miyawaki and Yamanaka in Yamanaka, stating that 'one of ordinary skill in the art would have been motivated to make such a combination in order to provide a way to synchronize operations for practical use [finding 4.18]'". Examiner agrees as explicit motivation is cited to establish obviousness (MPEP 2143.01).

Appellant then alleges that Yamanaka "is a solution based solely on a serial communications channel... problem with this approach is that the delay is not symmetrical nor is it consistent... there will be inherent inaccuracies based on the amount of message traffic on the serial communications channel... differs from the embodiments disclosed in the present application in that appellants use a discrete signal that all the processors receive

simultaneously... removes the delay and consequently any notion of having to adjust for it". The Examiner fails to see the relevance of the alleged difference as Appellant did not relate it to any claim limitation in order to distinguish the *claim language* from Yamanaka for patentability. Moreover, Examiner notes that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Appellant alleges that in Yamanaka, "neither the master nor the slave clocks synchronize or control operation of the CPU 10, typewriter 13, or typewriter controller 16 which the Examiner has construed as forming a document processing system". In response, the Examiner respectfully submits that CPU 10 is a common digital processing device that requires some kind of clocking control [i.e., master clock] in order to operate [i.e., synchronize data/instruction latching, processing, etc.]. The Examiner agrees with Appellant's admission on pages 15-16 of the instant Appeal Brief that "Yamanaka discloses... the master clock and slave clocks are synchronized so that status changes across the system can be arranged in a manner that is based on the time information", and relies upon Appellant's admission to establish that Yamanaka does teach synchronization between a controller [master] and resource [slave]. Moreover, the Examiner agrees with Appellant's admission on pages 16 of the instant Appeal Brief that Yamanaka discloses "CPU 10 records status changes of the slave stations... times of the slave clocks are also transmitted to the master station 1... arranges that data in sequence of time added acquisition of data from other slave stations during a constant period and then outputs such data to the typewriter 13", and relies upon Appellant's admission to establish that Yamanaka does teach the master clock [synchronized with slave clock in order to properly record time]

controlling the operation of the CPU [i.e., records status changes and arranges the data in sequence of time based on master clock] in order for the correct synchronized time to be recorded and arranged in the correct sequence of time. Thus, as demonstrated above, Yamanaka does disclose "the master [or] the slave clocks synchroniz[ing] or control[ling] operation of the CPU 10, typewriter 13, or typewriter controller 16 which the Examiner has construed as forming a document processing system".

Appellant concludes that "based on the foregoing, the explicit motivation to combine Miyawaki and Yamanaka identified by the Examiner... simply does not support combining any form of master/slave clock synchronization taught by Yamanaka with operation of any document processing system that may be taught by either Miyawaki *or Yamanaka*". Examiner disagrees and respectfully submits that the explicit motivation "to provide a way to synchronize operations for practical use" is applicable to the document processing system taught by Miyawaki. The resources of feeders/finishers disclosed by Miyawaki are independent modules that perform independent operations of transferring/receiving the sheets to/from the marking engine. However, Miyawaki did not discuss details of the essential synchronized operations amongst the independent modules [i.e., a transfer of sheet should be done before the copier actually imprints any image, and the imprinting should be completed before the sheet is to be received; if any of the operations are out of order, there would be no imprinted image on a sheet]. Therefore, one with ordinary skill in the art would have been motivated to look for a way to synchronize the operations amongst the independent modules for practical use [i.e., making successful copies]. As discussed previously, Examiner agrees with Appellant's admission on pages 15-16 of the instant Appeal Brief that "Yamanaka discloses... ***the master clock and slave clocks are***

synchronized so that status changes across the system can be arranged in a manner that is based on the time information". Appellant's admission is important in establishing that Yamanaka does teach synchronization between a controller [master] and resource [slave]. Due to the explicit motivation to provide a way to synchronize the copier operations for practical use, one with ordinary skill in the art would have used Yamanaka's teachings of clock synchronization in order to ensure that the copier operations of Miyawaki are performed in synchronized order according to a uniform synchronized time frame.

C. In the Alternative, Claims 1 3, 6, 7, 10, 11, and 21 Patentably Distinguish Over the Combination of Miyawaki and Yamanaka.

Appellant's arguments with respect to part C have been fully considered but they are not persuasive as detailed in the following.

In re rejection of claim 1 with finding 4.41, Appellant alleges that "the Miyawaki system bus 18 is not 'interconnecting the resource and the controller'". Firstly, Examiner disagrees as Miyawaki does teach the system comprising a control bus [system bus 18], interconnecting the resource [feeder, finisher; col.4, ll.8-11] and the controller [control unit; col.3, ll.54-63] [col.4, ll.35-39]. In detail, the control bus interconnects the resources and the controller through serial communication units 16, which acts as an interface to the resources. Secondly, Examiner is not aware of any explicit definition by the Appellant in the specification that restricts "interconnecting" to a direct connection without any interface.

In re rejection of claim 1 with findings 4.3-4.4, Appellant alleges that in Yamanaka, "neither the master nor the slave clocks synchronize or control operation of the CPU 10, typewriter 13, or typewriter controller 16 which the Examiner has construed as forming a

document processing system". As discussed above, the Examiner disagrees for the following reasons. First, Examiner respectfully submits that CPU 10 is a common digital processing device that requires some kind of clocking control [i.e., master clock] in order to operate [i.e., synchronize data/instruction latching, processing, etc.]. Second, Examiner agrees with Appellant's admission on pages 15-16 of the instant Appeal Brief that "Yamanaka discloses... the master clock and slave clocks are synchronized so that status changes across the system can be arranged in a manner that is based on the time information", and relies upon Appellant's admission to establish that Yamanaka does teach synchronization between a controller [master] and resource [slave]. Third, Examiner agrees with Appellant's admission on pages 16 of the instant Appeal Brief that Yamanaka discloses "CPU 10 records status changes of the slave stations... times of the slave clocks are also transmitted to the master station 1... arranges that data in sequence of time added acquisition of data from other slave stations during a constant period and then outputs such data to the typewriter 13", and relies upon Appellant's admission to establish that Yamanaka does teach the master clock [synchronized with slave clock in order to properly record time] controlling the operation of the CPU [i.e., records status changes and arranges the data in sequence of time based on master clock] in order for the correct synchronized time to be recorded and arranged in the correct sequence of time. Thus, as demonstrated above, Yamanaka does disclose "the master [or] the slave clocks synchroniz[ing] or control[ling] operation of the CPU 10, typewriter 13, or typewriter controller 16 which the Examiner has construed as forming a document processing system".

Appellant alleges that "moreover, the slave station 2 is not 'a resource that transfers the sheet to the marking engine or receives the sheet from the marking engine'... Yamanaka does

not disclose a 'resource' ... the Yamanaka data transmission path 5 is not interconnecting 'a resource that transfers the sheet to the marking engine or receives the sheet from the marking engine'... Yamanaka does not disclose a 'control bus' having the characteristics..." As discussed previously, Examiner respectfully submits that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. As indicated in part 6 of the Final Rejection, claims 1, 3, 6-7, 10-11, and 21 were rejected based on a combination of Miyawaki in view of Yamanaka. That is, the fact findings for Miyawaki [4.38-4.41] and Yamanaka [4.1-4.12], clearly written in claim language to match the pertinent limitations of claims 1, 3, 6-7, 10-11, and 21, demonstrate ***Miyawaki** is relied upon for teaching the details associated with a marking engine.* Moreover, Examiner is not aware of any teachings in either reference that teaches away from the combined whole.

In re rejection of claim 21, Appellant alleges that the "Examiner has not specifically identified any reference that discloses or fairly suggest the 'marking engine element of claim 21". Firstly, as indicated in part 6 of the Final Rejection, claims 1, 3, 6-7, 10-11, ***and 21*** were rejected based on ***a combination of Miyawaki in view of Yamanaka***. That is, the fact findings for Miyawaki [4.38-4.41] and Yamanaka [4.1-4.12], were clearly written in claim language to match the pertinent limitations of claims 1, 3, 6-7, 10-11, ***and 21***. Thus, Examiner respectfully submits that Examiner has specifically identified references [part 6 of the Final Rejection] that discloses or fairly suggest the "marking engine element of claim 21". Further, Examiner submits that claims 1 and 21 are practically identical except for a few limitations that are addressed by findings 4.2, 4.9, and 4.10. These findings were specifically cited in lieu of the others already cited in reference to claim 1 in order to pinpoint the particular distinction between the two claims

for ease of prosecution. To further support Examiner's position, Appellant's remaining allegation in the same paragraph on pages 20-21 of the instant Appeal Brief asserts "additionally, ***as discussed above in the arguments that distinguish claim 1*** from findings 4.3 and 4.4..." with the same allegations that were discussed above.

D. In the Alternative, Claim 2 Patentably Distinguishes Over the Combination of Miyawaki, Yamanaka, and Shimoda.

Appellant's arguments with respect to part D have been fully considered but they are not persuasive as detailed in the following.

In re rejection of claim 2, Appellant disagrees "as to findings 4.41, 4.3 and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3 and 4.4". As such, Examiner's positions against Appellant's allegations as discussed above are also applicable in this instance.

E. In the Alternative, Claims 4 and 8 Patentably Distinguish Over the Combination of Miyawaki, Yamanaka, and Lackman.

Appellant's arguments with respect to part E have been fully considered but they are not persuasive as detailed in the following.

In re rejection of claim 4, Appellant disagrees with finding 4.5 that "Yamanaka discloses the resource circuitry includes a processor... for adjusting the slave clock to provide compatibility with the controller" and supports the disagreement with the previous allegations "that distinguish claim 1 from findings 4.3 and 4.4...neither the master nor the slave clocks synchronize or control operation of the CPU 10, typewriter 13, or typewriter controller 16 which the Examiner has construed as forming a document processing system". In response, the

Examiner respectfully submits that CPU 10 is a common digital processing device that requires some kind of clocking control [i.e., master clock] in order to operate [i.e., synchronize data/instruction latching, processing, etc.]. The Examiner agrees with Appellant's admission on pages 15-16 of the instant Appeal Brief that "Yamanaka discloses... the master clock and slave clocks are synchronized so that status changes across the system can be arranged in a manner that is based on the time information", and relies upon Appellant's admission to establish that Yamanaka does teach synchronization between a controller [master] and resource [slave]. Moreover, the Examiner agrees with Appellant's admission on pages 16 of the instant Appeal Brief that Yamanaka discloses "CPU 10 records status changes of the slave stations... times of the slave clocks are also transmitted to the master station 1... arranges that data in sequence of time added acquisition of data from other slave stations during a constant period and then outputs such data to the typewriter 13", and relies upon Appellant's admission to establish that Yamanaka does teach the master clock [synchronized with slave clock in order to properly record time] controlling the operation of the CPU [i.e., records status changes and arranges the data in sequence of time based on master clock] in order for the correct synchronized time to be recorded and arranged in the correct sequence of time. Thus, as demonstrated above, Yamanaka does disclose "the master [or] the slave clocks synchroniz[ing] or control[ling] operation of the CPU 10, typewriter 13, or typewriter controller 16 which the Examiner has construed as forming a document processing system".

Appellant alleges that "moreover, the slave station 2 is not 'a resource that transfers the sheet to the marking engine or receives the sheet from the marking engine'... Yamanaka does not disclose a 'resource' ... the Yamanaka data transmission path 5 is not interconnecting 'a

resource that transfers the sheet to the marking engine or receives the sheet from the marking engine'... Yamanaka does not disclose a 'control bus' having the characteristics..." As discussed previously, Examiner respectfully submits that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. As indicated in part 6 of the Final Rejection, claims 1, 3, 6-7, 10-11, and 21 were rejected based on a combination of Miyawaki in view of Yamanaka. That is, the fact findings for Miyawaki [4.38-4.41] and Yamanaka [4.1-4.12], clearly written in claim language to match the pertinent limitations of claims 1, 3, 6-7, 10-11, and 21, demonstrates ***Miyawaki*** *is relied upon for teaching the details associated with a marking engine.* Moreover, Examiner is not aware of any teachings in either reference that teaches away from the combined whole.

Appellant concludes that "claim 4 depends from claims 1 and 3... therefore, Yamanaka does not disclose a 'resource circuitry' having the characteristics alleges by the Examiner in finding 4.5". Essentially, Appellant has reiterated the allegations above without specifically arguing in reference to finding 4.5 by distinguishing the claim language against the findings. As such, Examiner's positions against Appellant's allegations as discussed above are also applicable in this instance.

In re rejection of claim 8, Appellant has made the same arguments as he did with respect to claim 4. Thus, the Board's attention is directed to the discussion above for the Examiner's response to those arguments.

In addition, re claim 8, Appellant alleges that "furthermore, Yamanaka does not disclose 'resources' having the characteristics alleged in finding 4.13". Examiner disagrees as Yamanaka

does disclose a document processing system comprising a plurality of "resources" [slave stations 2 and 3] [col.7, ll.3-5].

Appellant alleges that "moreover, Lackman deals with a accessing a disk... it has nothing to do with synchronizing clocks between modules". In response to applicant's argument that Lackman is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Examiner submits that both Lackman [col.1, ll.6-14] and Appellant are associated with data processing systems [i.e., Appellant's processing system involves data] and that both Lackman and Appellant are involved with the problem of how to stop an operation in real time [findings 4.34-4.35].

F. *In the Alternative, Claim 12 Patentably Distinguishes Over the Combination of Miyawaki, Yamanaka, and Einbinder.*

Appellant's arguments with respect to part F have been fully considered but they are not persuasive as detailed in the following.

In re rejection of claim 12, Appellant has made the same arguments "that distinguish claim 1 from findings 4.3 and 4.4...neither the master nor the slave clocks synchronize or control operation of the CPU 10, typewriter 13, or typewriter controller 16 which the Examiner has construed as forming a document processing system" and that "the slave station 2 is not 'a resource that transfers the sheet to the marking engine or receives the sheet from the marking

engine'". Thus, the Board's attention is directed to the discussion above for the Examiner's response to those arguments.

In addition, Appellant concludes that "claim 12 depends from claims 1 and 6... therefore, Yamanaka does not disclose any 'resources' having the characteristics alleges by the Examiner in finding 4.6... the Yamanaka data transmission path 5 is not 'interconnecting the resources and the controller' as recited in claim 12... therefore, Yamanaka does not disclose a 'control bus' having the characteristics alleges by the Examiner in finding 4.7". Essentially, Appellant has reiterated the allegations above without specifically arguing in reference to finding 4.6 and 4.7 by distinguishing the claim language against the findings. As such, Examiner's positions against Appellant's allegations as discussed above are also applicable in this instance.

Further, Appellant alleges that "moreover, Einbinder deals with prioritizing which device can be accessed from other devices that are connected". In response to applicant's argument that Einbinder is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Examiner submits that both Einbinder [col.1, ll.5-10] and Appellant are associated with data processing systems [i.e., Appellant's processing system involves data] and that both Lackman and Appellant are involved with the problem of how to transfer data [findings 4.36].

Appellant alleges that Einbinder "never discusses anything about synchronization". As discussed previously, Examiner respectfully submits that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references.

As indicated in part 19 of the Final Rejection, claim 12 was rejected based on a combination of Miyawaki, Yamanaka and Einbinder with ***Yamanaka*** *being relied upon for teaching the details associated with synchronization.*

G. *In the Alternative, Claims 5 and 9 Patentably Distinguish Over the Combination of Miyawaki, Yamanaka, and Cheung.*

Appellant's arguments with respect to part G have been fully considered but they are not persuasive as detailed in the following.

In re rejection of claim 5, Appellant disagrees "as to findings 4.41, 4.3 and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3 and 4.4; as to finding 4.5 for the same reasons provided above that distinguish claim 4 from finding 4.5". As such, Examiner's positions against Appellant's allegations as discussed above are also applicable in this instance.

Appellant alleges that "in finding 4.21... this portion of Cheung [col.4, ll.37-41] does not disclose or fairly suggest that 'the slave clock is synchronized to within one clock cycle of the master clock'". Examiner submits that Cheung does teach the slave [Process A] clock synchronized to within one clock cycle [represented by interval between U-Q and U + Q + V- T] of the master clock [U of process B]. As indicated by Cheung [col.4, ll.37-41], the new time for the slave clock is within the interval between U-Q and U + Q + V- T, or an absolute time value of **2Q + V – T**, where Q represents the ***precision*** desired, T represents the first slave clock time and V represents the second slave clock time. As Appellant did not argue why the values of Q, V and T cannot be set appropriately as indicated by the Examiner in finding 4.21, Examiner

submits that the values of Q, V and T can be set appropriately so that the slave clock interval of **2Q + V – T** is synchronized to within one clock cycle of the master clock U.

Appellant alleges that "Cheung is a scheme that utilizes mathematics to better estimate what the average or best round trip time would be on a network... it is not based on having a separate discrete wire that is used to synchronize the processors... inherent delay because of message traffic applies". The Examiner respectfully submits that Cheung does not merely teach "a scheme that utilizes mathematics to better estimate what the average or best round trip time would be on a network", but actually utilizes the innovative scheme for synchronizing master and slave clocks [col.1, ll.8-12]. Moreover, the Examiner fails to see the relevance of the alleged differences as Appellant did not relate it to any claim limitation in order to distinguish the *claim language* from Cheung for patentability. The Examiner notes that although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

In re rejection of claim 9, Appellant disagrees "as to findings 4.41, 4.3 and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3 and 4.4; as to finding 4.5 for the same reasons provided above that distinguish claim 4 from finding 4.5; as to findings 4.8 and 4.13 for the same reasons provided above that distinguish claim 8 from findings 4.8 and 4.13; as to finding 4.21 for the same reasons provided above that distinguish claim 5 from finding 4.21". As such, Examiner's positions against Appellant's allegations as discussed above are also applicable in this instance.

H. *In the Alternative, Claims 13-20 Patentably Distinguish Over the Combination of Miyawaki, Yamanaka, and Cheung.*

Appellant's arguments with respect to part H have been fully considered but they are not persuasive as detailed in the following.

In re rejection of claim 13, Appellant disagrees "as to findings 4.41, 4.3 and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3 and 4.4; as to finding 4.13 for the same reasons provided above that distinguish claim 8 from finding 4.13". As such, Examiner's positions against Appellant's allegations as discussed above are also applicable in this instance.

Appellant alleges that "in findings 4.16 and 4.17... however, as described above in distinguishing claim 1 from findings 4.3 and 4.4... therefore, Yamanaka does not disclose a 'resource' having the characteristics alleged by findings 4.16 and 4.17". As discussed previously, Examiner respectfully submits that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. As indicated in part 21 of the Final Rejection, claims 5, 9, and 13-20 were rejected based on a combination of Miyawaki, Yamanaka, and Cheung to disclose each and every limitation. Moreover, Appellant did not argue specifically in reference to finding 4.16 and 4.17 by distinguishing the claim language against the findings. Instead, Appellant has reiterated the allegations above in reference to finding 4.3 and 4.4. As such, Examiner's positions against Appellant's allegations as discussed above are also applicable in this instance.

Appellant alleges that "in findings 4.24 and 4.29... however, Cheung does not disclose or fairly suggest operation of 'a resource that transfers the sheet to the marking engine or receives the sheet from the marking engine'... therefore, Cheung does not disclose a 'resource' having the characteristics alleged by findings 4.24-4.29". As discussed previously, Examiner

respectfully submits that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. As indicated in part 21 of the Final Rejection, claims 5, 9, and 13-20 were rejected based on a combination of Miyawaki, Yamanaka, and Cheung to disclose each and every limitation.

Appellant alleges that "furthermore, in finding 4.24... claim 13 is distinguished from the portion of Cheung cited by the Examiner because Process B (relating to the controller) does not save a value of its clock until after it receives the message from Process A (allegedly relating to the resource)... therefore, Cheung does not disclose the method alleged by finding 4.24". Examiner references finding 4.24 citing Cheung, col.4, ll.8.10, which states "Process A sends a message (4) to Process B, which receives the message some time later... B then obtains a ***time stamp***, from its local clock". Obtaining a time stamp is akin to one going to the post office and getting a time stamped on your mail. A notary looks at what current time is being indicated [i.e., saved] and notarizes the time accordingly. Similarly, Process B [controller] obtains a time stamp by going to a time counter and retrieves the current time that's saved in the time counter. Thus, Examiner submits that Cheung does disclose the method of finding 4.24.

Appellant alleges that "additionally, in finding 4.29... notably, Cheung teaches dividing the difference between first and second slave clock values by two which is ***not required*** in the claimed method... therefore, Cheung does not disclose the method alleged by finding 4.29". Examiner submits that claim 13 cites "a method... ***comprising*** the steps of". Hence, the claimed method uses open language that does not preclude other steps that may be present in Cheung [e.g., dividing the difference between first and second slave clock values by two].

In re rejection of claim 14, Appellant disagrees "as to findings 4.41, 4.3 and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3 and 4.4; as to finding 4.13 for the same reasons provided above that distinguish claim 8 from finding 4.13; as to finding 4.16 and 4.17 for the same reasons provided above that distinguish claim 13 from finding 4.16 and 4.17; as to findings 4.19 and 4.24-4.29 for the same reasons provided above that distinguish claim 13 from findings 4.19 and 4.24-4.29". As such, Examiner's positions against Appellant's allegations as discussed above are also applicable in this instance.

In re rejection of claim 15, Appellant disagrees "as to findings 4.41, 4.3 and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3 and 4.4; as to finding 4.13 for the same reasons provided above that distinguish claim 8 from finding 4.13; as to finding 4.16 and 4.17 for the same reasons provided above that distinguish claim 13 from finding 4.16 and 4.17; as to findings 4.19 and 4.24-4.29 for the same reasons provided above that distinguish claim 13 from findings 4.19 and 4.24-4.29". As such, Examiner's positions against Appellant's allegations as discussed above are also applicable in this instance.

Appellant alleges that "in finding 4.30... notably, Cheung teaches dividing the difference between first and second slave clock values by two which is ***not required*** in the claimed method... therefore, Cheung does not disclose the method alleged by finding 4.30". Examiner submits that claim 15 cites "a method... ***comprising*** the steps of". Hence, the claimed method uses open language that does not preclude other steps that may be present in Cheung [e.g., dividing the difference between first and second slave clock values by two].

In re rejection of claim 16, Appellant disagrees "as to findings 4.41, 4.3 and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3 and 4.4; as to

finding 4.5 for the same reasons provided above that distinguish claim 4 from finding 4.5; as to findings 4.19 and 4.24-4.29 for the same reasons provided above that distinguish claim 13 from findings 4.19 and 4.24-4.29; as to finding 4.21 for the same reasons provided above that distinguish claim 5 from finding 4.21". As such, Examiner's positions against Appellant's allegations as discussed above are also applicable in this instance.

In re rejection of claim 18, Appellant alleges that "in finding 4.31... notably, Cheung teaches dividing the difference between first and second slave clock values by two which is ***not required*** in the claimed method... therefore, Cheung does not disclose the method alleged by finding 4.31". Examiner submits that claim 18 depended from claims 15 and 17 cites "a method... ***comprising*** the steps of': Hence, the claimed method uses open language that does not preclude other steps that may be present in Cheung [e.g., dividing the difference between first and second slave clock values by two].

In re rejection of claim 19, Appellant disagrees "as to findings 4.41, 4.3 and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3 and 4.4; as to finding 4.13 for the same reasons provided above that distinguish claim 8 from finding 4.13; as to finding 4.16 and 4.17 for the same reasons provided above that distinguish claim 13 from finding 4.16 and 4.17; as to findings 4.19 and 4.24-4.29 for the same reasons provided above that distinguish claim 13 from findings 4.19 and 4.24-4.29; as to finding 4.32 for the same reasons provided above that distinguish claim 13 from finding 4.32". As such, Examiner's positions against Appellant's allegations as discussed above are also applicable in this instance.

In re rejection of claim 20, Appellant disagrees "as to findings 4.41, 4.3 and 4.4 for the same reasons provided above that distinguish claim 1 from findings 4.41, 4.3 and 4.4; as to

finding 4.5 for the same reasons provided above that distinguish claim 4 from finding 4.5; as to findings 4.8 and 4.13 for the same reasons provided above that distinguish claim 8 from findings 4.8 and 4.13; as to finding 4.21 for the same reasons provided above that distinguish claim 5 from finding 4.21". As such, Examiner's positions against Appellant's allegations as discussed above are also applicable in this instance.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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